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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/502,675	02/11/2000	Shunpei Yamazaki	0756-2101	5514

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EXAMINER
PERT, EVAN T

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 04/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/502,675	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Evan T. Pert	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44 and 81-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44 and 81-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *14 January 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *13* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The proposed corrections to the drawings were received on 1-14-02. These drawings are approved.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-44 and 81-85 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicants regard as their invention.

Evidence that claims 1-44 fail to correspond in scope with that which applicants regard as the invention can be found in Paper No. 13 filed 1/14/02. In that paper, on page 8, applicant has stated that:

> the essence of the present invention is to optimize the structure of TFTs that constitutes each circuit in response to the respective specifications of the pixel portion and the driver portion, by providing the LDD region so as to be overlapped, partially overlapped, or non-overlapped with the gate electrode.

Applicant explains that "the essence" of the invention includes *five* types of transistors of a "structure" that is optimized cooperatively among the five types of transistors. This statement at page 8 of paper no. 13 indicates that the invention is different from what is defined in the claims because applicant's invention defined in the claims does not include the "**5** types of transistors".

Applicant argues that an "optimization among five types of transistors" is the basis for distinguishing from what would be an obvious use of "GOLD" (gate over-lapped drain) transistors (as taught by Hatano) in the driver circuitry of AAPA, for the "high speed", "hot carrier immunity" and "system-on-display" advantage taught by Hatano, as has been set forth on record in paper no. 11.

While applicant's statement that the "essence" of applicant's invention includes a cooperative optimized relationship among *five* types of transistors in driver and pixel circuitry, the scope of applicant's claims reaches in other directions.

For example, claims 1-8 recite a "first", "fourth" and "fifth" transistor, but are silent about a "second" and "third" transistor. Yet, based on applicant's statement in paper no. 8, the "essence" of applicant's invention includes *five* transistors, optimized for operation *together*.

In claims 9-17, a "third" transistor is never mentioned, but "first", "second", "fourth" and "fifth" transistors *are* mentioned.

In claims 18-26, "third", "fourth" and "fifth" transistors are recited, but nothing is mentioned about a "first" and "second" transistor.

In claims 27-35, only "first", "second" and "fourth" transistors are recited.

In claims 36-44, only two transistors are recited except in claims 39-44 where a 4^{th} transistor having no antecedent basis is recited.

The examiner notes that the transistors "missing" from claims 1-44 might even arguably raise a question of *indefiniteness* since one might presumably wonder "are these missing transistors optional?" Will they be invented or added *later*? What do they look like?

However, the examiner interprets the "first", "second", "third", "fourth" and "fifth" transistors based on the cooperative relationship consistently set forth within the specification.

The examiner respectfully submits that "the essence" of applicant's invention *requires* 5 transistors optimized and interrelated as *evidenced* by applicant's statement on page 8 of paper no. 13.

3. Claims 39-44 recite the limitation "fourth transistor". There is insufficient antecedent basis for this limitation in the claims since applicant cancelled "fourth transistor" from claim 36 in paper no. 13.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 9, 18, 27, 36 and 81-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in view of Hatano et al. (IEEE article).

Hatano teaches n-type transistors for the GOLD structure. It would have been obvious to one of ordinary skill in the art at the time of applicant's claimed invention to choose n-channel TFTs for those TFTs demanding higher switching speed and resistance to hot carrier effects. Hatano teaches n-type "third" impurity region as the "n-" extension region in Fig. 4, which is n-type. In choosing n-type for the transistors requiring faster switching, the complementary p-type devices of AAPA would be obvious in view of the necessary functional operation of CMOS.

AAPA sets forth the previous existence of driver circuitry having sampling and shift register circuits requiring higher speed, and pixel circuitry having LDD structures "outside the gate electrode" all on the same substrate wherein there are different demands, electrically, placed on the various circuits [pages 1-6 of specification].

The independent claims cite up to five different transistors wherein p-type and n-type transistors constitute driver CMOS having GOLD (gate overlapped LDD) structures, and the pixel circuits constitute only one conductivity type transistor in the actual pixel area, these having ordinary LDD.

The examiner refrains from using the "first, second, third, fourth, and fifth transistor" language as well as the "a conductivity type" and "an opposite conductivity type" language as these are more difficult to follow. Since "channel forming regions" and "impurity regions" are inherent to TFTs, with n-type and p-type impurities available, engineers do not speak of "first" and "second" regions, but speak in language as in the statement on page 8 of paper no. 13 where applicant explains the essence of the invention as being the optimization of five transistors.

It has long been well known that there are two types of semiconductor conductivity known as p-type and n-type, together forming CMOS, the driver circuitry explained by AAPA. There are many transistors requiring different characteristics. Particularly, the higher-speed peripheral driver circuits are limiting when they cannot scan as fast as needed, for example.

Hatano et al. recognize the need for a GOLD (gate overlapped LDD) process in TFTs that form a "system-in-display", where the driver CMOS and pixel circuitry is on the same insulating substrate [Introduction].

It would have been obvious for one of ordinary skill in the art to modify the structure of AAPA to include the Sa-GOLD TFTs taught by Hatano et al.. One of ordinary skill in the art would be motivated to include these in the higher voltage and higher speed driver circuits of the AAPA, at the suggestion of Hatano et al., to attain "high immunity against hot-carrier stress" [Conclusion].

Regarding claims 8, 17, 26, 35 and 44, it is obvious for anyone of ordinary skill in the art that a display is useful in a wide range of consumer products enumerated as "limitations". The examiner emphasizes that it is not at all surprising to apply TFT displays to consumer products because consumers demand the types of products enumerated by these claims.

6. Claims 2, 10-11, 19-20, 28-29 and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Hatano et al. as applied to claims 1, 9, 18, 27 and 36 above, and further in view of Mimura et al. (U.S. 6,127,210).

Regarding claim 19, the claim does not specify any location of a "second impurity region having a length of 0.5 to 3.0 um", so it could be the source and drain region, which is commonly in the range of 0.5 to 3.0 um. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to adjust the size of the second impurity region to gain easier access for making contact to the source and drain, for example.

Regarding claims 20 and 27, it would have been obvious to one of ordinary skill in the art to adopt sampling circuits and shift register circuits taught in AAPA since data needs to be samples for delivery to pixel areas and drivers are needed to deliver the sampled data to the pixel portions.

Mimura et al. teach a method of forming CMOS TFT circuitry that involves dopant "compensation" as a way to reduce the number of masking steps required. As a result, the device regions having impurities for LDD and source/drain structures contain both n-type and p-type dopant, with the greater concentration setting the dopant type, the dopant type being either "n-type or p-type" (or "intrinsic" when n and p are equal).

It would have been obvious to adopt the method of Mimura et al. in using dopant "compensation" to result in a structure having both minority and majority dopant.

7. Claims 3-4, 12-13, 21-22, 30-31, 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Hatano et al. as applied to claims 1, 9, 18, 27 and 36 above, and further in view of Mikoshiba (U.S. 5,499,123).

Mikoshiba teaches a light-shielding layer 312 with oxidization to form insulating layer 314 on the light shield with overlap of the pixel electrode308 defining a capacitance. Mikoshiba teaches at least aluminum with aluminum oxide and tantalum with tantalum oxide.

It would have been obvious to adopt the method of Mikoshiba to get a good capacitor for the pixel. The oxidized light-shielding layer offers a good dielectric, as explained by Mikoshiba as a motivation for using his invention.

8. Claims 5-7, 14-16, 23-25, 32-34 and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Hatano et al. taken with Mikoshiba, as applied to claims 3, 12, 21, 30 and 39 above, and further in view of Fukunaga et al. (U.S. 5,706,064).

Fukunaga et al. teach the benefits of an organic-inorganic hybrid glass layer at the capacitor dielectric in a TFT display, motivating one of ordinary skill in the art to implement the obvious improvement of using a laminate of organic and inorganic layers for increased reliability [Summary of Invention].

9. Claims 81-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Hatano et al. as applied to claim1, 9, 18, 27 and 36 above, and further in view of Stewart.

Stewart teaches TFT EL displays. It would have been obvious to incorporate the GOLD process taught by Hatano et al. to make EL displays because the driver circuitry in EL displays must also be higher than the pixel circuitry, in making a "system--in-display" at the suggestion of Hatano.

Response to Arguments

10. Applicant's arguments filed 1-14-02 have been fully considered but they are not persuasive. Applicant argues that the rejection of record under 35 USC 103 is improper since "the essence of applicant's invention" distinguishes from the obvious use of Hatano's GOLD structure in AAPA CMOS shift register and sampling circuit system-on-display circuitry. Applicant argues that the various over-lapping or non-overlapping LDD regions *of five types of transistors* distinguish from the prior art.

Yet, pending claims 1-44 and 81-85 do not actually specify any particular overlapping except for some "third" impurity region which must be inside the gate region for a transistor in a CMOS driver circuit, and this is only for claims 1-17 and 27-35.

The "first" impurity region in claims 1-35 is simply "outside the gate region", but could be inside also. The "second" impurity region could be located *anywhere* by the recitation in claims 1-44. The "fourth" impurity region could also be *anywhere* by the recitation in claims 1-44.

In fact the relationship among the "first", "second", "third", "fourth" and "fifth" impurity regions and "first", "second", "third", "fourth" and "fifth" transistors defined in the claims is potentially confusing without *careful* reading in full view of the light of the specification. Since applicant has "optimized" the five transistors for operation together, as "the essence" of the invention, applicant is required to clearly and distinctly claim that which applicant regards as applicant's invention. To date, applicant has not met this requirement.

In summary, applicant's failure to distinctly claim what applicant regards as applicant's invention permits the vaguely defined claims to "read on" the obvious use of GOLD structure transistors in the CMOS driver circuitry of an AAPA system-on-display, at the suggestion of Hatano et al..

Conclusion

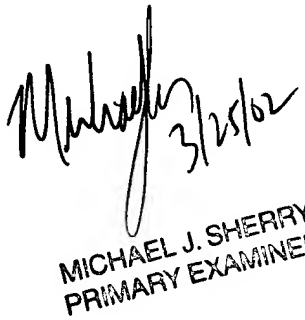
11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan T. Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 703-308-1680. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



ETP
March 24, 2002